AMENDMENTS TO THE SPECIFICATION

In the Specification:

Please replace the paragraph beginning on page 12, line 10 as follows:

The first semiconductor active layers 11r, 11g, and 11b and the second semiconductor active layers 21r, 21g, and 21b may be formed, for example, of a thin layer of polycrystalline silicon. As described above, the second semiconductor active layers 21r, 21g, and 21b are arranged in different directions for R, G, and B sub-pixels. To be more specific, it is the channel regions at the centers of the second semiconductor active layers 21r, 21g, and 21b that can have different directions. However, FIG. 1 shows the arrangement of the second semiconductor active layers in their entirety in different directions ~~in order~~ to avoid ~~unnecessarily~~ ~~complicate~~ complicating the drawing unnecessarily. Hence, the arrangement directions of TFT active layers will replace the arrangement directions of channel regions of the TFT active layers, as it is the channel regions of TFT active layers, not the TFT active layers in their entirety, which can be arranged in different directions. This fact will refer equally to all embodiments to be described later.

Please replace the paragraph beginning on page 19, line 7 as follows:

As shown in FIG. 5, the second semiconductor active layer 21r is disposed such that the current-flowing direction at a channel region C1 is approximately parallel to the side grain boundaries 62, that is, the direction of current-flow in the channel region C1 makes about 90 degrees with the primary grain boundaries 61. The second semiconductor active layer 21g is disposed such that the direction of current-flow in a channel region C2 is perpendicular to the side grain boundaries 62, that is, the current-flowing direction at the channel region C2 makes about 0 degrees with the primary grain boundaries 61. The second semiconductor active layer

21B is disposed such that the direction of current-flow in a channel region C3 is inclined with respect to ~~the side grain boundaries 62, that is,~~ the primary grain boundaries 61.

Please replace the paragraph beginning on page 22, line 14 as follows:

The charging capacitor 30 is located between the first and second TFTs 10 and 20 and stores the amount of driving voltage necessary to drive the second TFT 20, for a period of one frame. As can be seen from FIGS. 6 and 8, the capacitor 30 can be made up of first and second electrodes 31 and 32 and an inter-insulating layer 4. The first electrode 31 is connected to the drain electrode 15 of the first TFT 10. The second electrode 32 overlaps the first electrode 31 and is electrically connected to a driving line 53, which is a power applying line, via a power line electrode 33. The inter-insulating layer 4 is formed between the first and second electrodes 31 and 32 and is used as a dielectric. The structure of the charging capacitor 30 is not limited to the structure shown in FIG. 8. For example, a silicon thin film for the TFT 10 and a conductive layer of the gate electrode 13 can be used as the first and second electrodes 31 and 32, respectively, and the gate insulating layer 3 can be used as a dielectric layer. Various other methods can also be used.